What is claimed is:

1. An apparatus for displaying an image corresponding to a digital image file, comprising:
    a) an image processing memory portion, the image processing memory portion including an image buffer for the computation of an image from a digital image file;
    b) an integrated circuit in communication with the image processing memory portion, the circuit including integrated processing capability for the computing of a the image corresponding to the digital image file; and
    c) a video memory portion in communication with the circuit, the video memory portion being capable of storing a plurality of computed images that are computed by the circuit.

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2. The apparatus of claim 1, further comprising a control processing unit that is capable of providing one or more of:
    a) file system processing operations directed to a storage device or interface that provides the digital image file;
    b) parsing, interpretation, and validation of compressed image file headers;
    c) interpretation and execution of user commands; and
    d) coordination of image processing operations of the integrated circuit.

3. The apparatus of claim 1, further comprising a non-volatile memory portion that contains executable program code defining one or more operational characteristics of the apparatus or of a device into which the apparatus is incorporated, and that also contains one or more images used for informational or background display purposes.

4. The apparatus of claim 1, further comprising a direct memory access controller that is capable of providing efficient data transfer to or from the media or interfaces that provide the digital image files to the apparatus, the image processing memory portion, the integrated circuit, and the video memory portion.

5. The apparatus of claim 1, further comprising one or more SDRAM controllers that provide control memory initialization, read and write cycles, and refresh operations.

6. The apparatus of claim 1, further comprising at least one bus arbitration and multiplexing logic device that allows the image processing memory portion, the video memory portion, the integrated circuit, and file storage media to share one or more common signals.

7. The apparatus of claim 1, wherein the integrated processing capability includes converting the digital image file into a viewable bitmapped image.

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8. The apparatus of claim 7, wherein the integrated processing capability further includes rescaling the viewable bitmapped image to fit an available viewing area of a television display.

9. The apparatus of claim 7, wherein the integrated processing capability further includes filtering the viewable bitmapped image to reduce the severity of at least one television display artifact selected from the group consisting of cross-luminance, cross-chrominance, and video flicker.

10. The apparatus of claim 7, wherein the integrated processing capability further includes converting the viewable bitmapped image into a television video signal.

11. The apparatus of claim 1 further comprising an output that is capable of delivering any of the plurality of computed images to a display device without performing further digital computation.

12. The apparatus of claim 11, wherein the processor is capable of providing time-multiplexed image data and one or more video synchronization signals to form a composite video signal.

13. The apparatus of claim 1, wherein the integrated circuit is an application-specific integrated circuit or a field programmable gate array.

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14. The apparatus of claim 1, wherein the apparatus is further capable of decoding, storing, and providing informational or background images for delivery to a video output or display device.

15. The apparatus of claim 1, wherein the circuit is further capable of transferring a computed image from the image processing memory portion to the video memory portion.

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16. The apparatus of claim 15, wherein the circuit is further capable of delivering one or more synchronization pulses to a video output or display device via the video processor when the computed image is being transferred from the image processing memory portion to the video memory portion.

17. The apparatus of claim 1, wherein the apparatus is further capable of inserting phase compensation pixels in between video frames so that an identical subcarrier phase is established in consecutive video frames.

18. The apparatus of claim 1 wherein the circuit is further capable of providing one or more of picture-in-picture video insertion, split-image display, and image transition effects.

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19. The apparatus of claim 1 wherein the circuit is further capable of providing an image navigation function, whereby the circuit increments or decrements an image index counter in response to user commands.

20. The apparatus of claim 1 wherein the circuit is further capable of managing images cached in the video memory portion in a manner consistent with the direction of navigation as expressed by a user of the apparatus.

21. A method of processing a digital image file, comprising:

a) receiving a first compressed image file corresponding to a first still picture;

b) creating, using a processor and an image processor memory buffer, a first decompressed image file corresponding to the first compressed image file;

c) converting the first decompressed image file to a first composite video signal;

d) transferring the composite video signal to a video memory buffer; and

e) delivering the composite video signal to a display device or video output.

22. The method of claim 21 wherein the transferring step includes storing the first decompressed image file in solid-state memory.

23. The method of claim 21 wherein the converting step includes at least one of:

a) rescaling the first decompressed image file in a horizontal dimension to correspond to a number of visible horizontal pixels on a television display;

b) filtering the first decompressed image file in a horizontal dimension to reduce chrominance bandwidth and associated video cross-luminance artifacts;

c) filtering the first decompressed image file in a horizontal dimension to reduce luminance bandwidth and associated video cross-chrominance artifacts;

d) rescaling the first decompressed image file in a vertical dimension to correspond to a number of visible scanlines on a television display;

e) filtering the first decompressed image file in a vertical dimension to reduce inter-frame flicker;

f) rotating the picture associated with first decompressed image file in response to a user command; and

g) converting the first decompressed image file into a first chrominance-modulated video signal using digital computation methods including luminance gain scaling, luminance level offset, chrominance gain scaling, and chrominance quadrature modulation.

24. The method of claim 21 wherein the converting step comprises converting the first decompressed image file to a corresponding analog signal using a digital-to-analog converter circuit and lowpass filter.

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25. The method of claim 21 further comprising:

    a) receiving at least one additional compressed image file corresponding to at least one additional still picture; and

    b) creating, using the processor and the image processor memory buffer, at least one additional decompressed image file corresponding to the at least one additional compressed image file.

26. The method of claim 25 further comprising transferring the at least one additional decompressed image file to independent memory locations within the video memory portion.

27. The method of claim 21, wherein the delivering step comprises delivering the composite video signal to the display device or video output in a picture-in-picture or split-screen format.

28. An electronic device, comprising:

    a) a digital media reader capable of reading a plurality of compressed image files;

    b) an image processor and image processing memory portion capable of, in combination, computing an image corresponding to each of the compressed image files; and

    c) a video memory portion that is separate from the image processing memory portion and capable of storing computed images.

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29. The device of claim 28, further comprising one or more control switches for controlling operational aspects of the device.

30. The device of claim 28, further comprising visual indicators for alerting a user of an operational status of the device.

31. The device of claim 28, further comprising an infrared or other wireless receiver for receiving signals from a remote control transmitter.

32. The device of claim 28, further comprising an infrared or wireless remote control device.

33. The device of claim 32, wherein the remote control device contains one or more of:

a) a button that, when activated, causes a next image in sequence to be displayed;

b) a button that, when activated, causes a previous image in sequence to be displayed

c) a button that, when activated, causes the device to be enabled or disabled;

d) a button that, when activated, causes the device to enter an automatic slideshow mode; and

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e) a button that, when activated, causes the current displayed image to be rotated

34. The device of claim 28, further comprising a video bypass circuit capable of passing a video signal to the display device.

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